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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/711,224	09/02/2004	Paul A. Hyde	BUR920030186US1	5223

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EXAMINER	
CHARIOUI, MOHAMED	
ART UNIT	PAPER NUMBER
2857	

NOTIFICATION DATE	DELIVERY MODE
02/26/2008	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

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Office Action Summary	Application No.	Applicant(s)	
	10/711,224	HYDE ET AL.	
	Examiner	Art Unit	
	MOHAMED CHARIOUI	2857	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 November 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-35,37-46 and 54-57* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-18,24-35,37-44 and 54-57* is/are rejected.

7)☒ Claim(s) *19-23,45 and 46* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *21 November 2007* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

2. Applicant cancelled claims 36, 47-53, 58 and 59.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1-18, 24-35, 37-44 and 54-57 are rejected under 35 U.S.C. 102(e) as being anticipated by Joshi et al. (U.S. Patent Number 7,176,508)

The applied reference has a common Assignee with the instant application. Based upon the earlier effective U.S. filing date of the reference, it constitutes prior art under 35 U.S.C. 102(e). This rejection under 35 U.S.C. 102(e) might be overcome

either by a showing under 37 CFR 1.132 that any invention disclosed but not claimed in the reference was derived from the inventor of this application and is thus not the invention "by another," or by an appropriate showing under 37 CFR 1.131.

As per claim 1, Joshi et al. teach thermally coupling a first heating device to a first sensing device, generating heat at the first heating device (see col. 5, lines 24-36), measuring a change in at least one electrical characteristic of the first sensing device caused by the heat generated at the first heating device and calculating a temperature of the first heating device using the measured change in the at least one electrical characteristic (see col. 2, lines 55-67).

As per claim 2, Joshi et al. further teach that the calculating step is further based on a temperature versus power level relationship for the first heating device using the measured change in the at least one electrical characteristics of the of the first sensing device at different power levels and different distances from the first heating device (see col. 2, lines 55-67 and col. 4, lines 53-67).

As per claim 3, Joshi et al. further teach that the at least one electrical characteristic is a sub-threshold voltage slope (see col. 5, line 55 to col. 6, line 6).

As per claim 4, Joshi et al. further teach measuring a series of measurements between the first sensing device and the first heating device at varying amounts of power applied to the first heating device (see col. 6, lines 32-35).

As per claim 5, Joshi et al. further teach that the measuring step includes measuring a series of measurements between the first sensing device and the first heating device at varying distances (see col. 3, lines 48-53).

As per claim 6, Joshi et al. further teach that the first heating device and the first sensing device are a field effect transistor (see col. 2, lines 55-67).

As per claim 7, Joshi et al. further teach that the at least one electrical characteristic comprises drain current versus gate bias voltage (see col. 5, line 55 to col. 6, line 6).

As per claim 8, Joshi et al. further teach that the at least one electrical characteristic comprises sub-threshold voltage slope swing (see col. 5, line 55 to col. 6, line 6).

As per claim 9, Joshi et al. further teach thermally coupling the first heating device to the first sensing device is through silicon and comprises thermally coupling the first heating device to the first sensing device through a prescribed length of silicon (see col. 2, lines 55-67; col. 5, lines 24-36; and col. 6, lines 35-67).

As per claim 10, Joshi et al. further teach that the thermally coupling is a distance between about 0.01 to about 5 μm (see col. 6, line 35 to col. 7, line 26).

As per claim 11, Joshi et al. further teach that calibrating the first sensing device by measuring a particular electrical characteristic of an active region of the first sending device held at a known ambient temperature (see col. 7, lines 26-42).

As per claims 12 and 13, Joshi et al. further teach that the first sensing device is held at a known temperature and a sub-threshold voltage slope is measured incrementally in a range from 0-0.4 volts driving voltage of the first sensing device (see col. 5, line 55 to col. 6, line 25).

As per claim 14, Joshi et al. further teach generating heat at the first heating device comprises generating a substantially steady state heating, and measuring a change in at least one electrical characteristic of the first sensing device caused by the heat generated at the first heating device comprises measuring a substantially steady state change in the at least one electrical characteristic (see col. 2, lines 55-67).

As per claim 15, Joshi et al. further teach measuring a change in the at least one electrical characteristic of the first sensing transistor at room temperature (see col. 7, lines 25-33).

As per claim 16, Joshi et al. further teach that generating heat at the first heating device comprises running a current through the first heating device (see col. 2, lines 55-67).

As per claim 17, Joshi et al. further teach thermally coupling the first heating device to a second sensing device through silicon and measuring a change in at least one electrical characteristic of the second sensing device caused by the heat generated at the first heating device. (see col. 2, lines 55-67).

As per claim 18, Joshi et al. further teach thermally coupling a second heating transistor to a second sensing transistor through silicon; generating heat at the second heating transistor; and measuring a change in at least one electrical characteristic of the second sensing transistor caused by the heat generated at the second heating transistor (see col. 2, lines 55-67 and col. 3, line 64 to col. 4, line 15).

As per claim 24, Joshi et al. further teach that the measurement step includes providing a measurement differential taken with the first heating device and a second heating device having a different number of contacts (see col. 4, lines 35-52).

As per claim 25, Joshi et al. further teach thermally coupling a heating transistor to a measurement transistor at one or more predetermined distance (see col. 5, lines 24-36 and col. 6, line 35 to col. 7, line 10), calibrating the measurement transistor by measuring a particular electrical characteristic of an active region of the measurement transistor with the measurement transistor held at a known temperature (see col. 5, lines 1-10); generating heat at the heating transistor (see col. 5, lines 24-35); incrementally measuring a change in the at least one electrical characteristic of the measurement transistor caused by the heat generated at the heating transistor; and calculating a temperature of the heating transistor using the measured change in the at least one electrical characteristic (see col. 2, lines 55-67).

As per claim 26, Joshi et al. further teach that the calculating step is further based on a temperature versus power level relationship for the heating transistor based on an extrapolated form fitting curve (see col. 5, lines 36-55).

As per claim 27, Joshi et al. further teach that the calculating step is further based on using measured change in the at least one electrical characteristics of the of the first measurement transistor at different power levels and different distances from the heating transistor (see col. 6, line 35 to col. 7, line 10).

As per claim 28, Joshi et al. further teach that the at least one electrical characteristic is at least one of a sub-threshold voltage slope, drain current versus gate

bias voltage and a sub-threshold voltage slope swing (see col. 5, line 37 to col. 6, line 6).

As per claim 29, Joshi et al. further teach that the measuring step includes measuring a series of measurements between the measurement transistor and the heating transistor at varying distances (see col. 5, lines 24-36 and col. 6, line 35 to col. 7, line 10).

As per claim 30, Joshi et al. further teach that thermally coupling the heating transistor and the measurement transistor is through silicon and comprises thermally coupling the heating transistor to the measurement transistor through a prescribed length of silicon (see col. 5, lines 24-36).

As per claim 31, Joshi et al. further teach that the calibrating step includes the measurement transistor being held at a known temperature and a sub-threshold voltage slope is measured incrementally in a range from 0-0.4 volts driving voltage of the first sensing device (see col. 5, line 55 to col. 6, line 25).

As per claim 32, Joshi et al. further teach that the calibrating step includes determining a variation of at least one of the electrical characteristics of the measurement transistor as a function of temperature (see col. 5, lines 1-10).

As per claim 33, Joshi et al. further teach that the calibrating step is taken at various distances between the measurement transistor and the heating transistor (see col. 5, lines 1-10 and col. 6, line 35 to col. 7, line 10).

As per claim 34, Joshi et al. teach a silicon island (see col. 2, lines 55-67), and at least one pair of transistors, each pair of the at least one pair of transistors comprises a transistor configured to generate heat and a transistor configured to sense temperature (see col. 4, lines 1-15 and col. 4, lines 36-67), the transistor configured to generate heat and the transistor configured to sense temperature being arranged on the silicon island (see col. 4, lines 40-67); and a common source contact being arranged on the silicon island and leading to the source of both the transistor configured to generate heat and the transistor configured to sense temperature (see col. 4, lines 1-30 and col. 4, lines 40-67), wherein each transistor of each pair of transistors is arranged a prescribed distance from its corresponding transistor (see col. 6, line 35 to col. 7, line 10).

As per claim 35, Joshi et al. further teach that the prescribed distance ranges from about 0.1 μm to about 5 μm (see col. 6, line 35 to col. 7, line 10).

As per claim 37, Joshi et al. further teach that the transistor configured to generate heat is configured to have a current selectively run through it, and the transistor configured to sense temperature is configured to produce a change in at least one of electrical characteristic of the transistor configured to sense temperatures, the change is proportional to heat generated by the transistor configured to generate heat (see col. 2, lines 55-67).

As per claim 38, Joshi et al. further teach a circuit to sense the change in the at least one electrical characteristic (see col. 2, lines 55-67).

As per claim 39, Joshi et al. teach at least one silicon island (see col. 2, lines 55-67); at least one heating field effect transistor configurable to generate heat arranged within the silicon island; at least one sensing field effect transistor arranged within the at least one silicon island corresponding to each heating field effect transistor of the at least one heating field effect transistor, wherein each sensing field effect transistor is arranged a prescribed distance from its corresponding heating field effect transistor and each sensing field effect transistor is configurable to sense a temperature (see col. 6, line 35 to col. 7, line 10); and means to calculate a temperature of the each heating field effect transistor using a measured change in at least one electrical characteristic of the each sensing field effect transistor caused by the heat generated at the each heating field effect transistor (see col. 2, lines 55-67).

As per claim 40, Joshi et al. further teach that the at least one silicon island is at least partially surrounded by an insulator (see col. 6, lines 14-25).

As per claim 41, Joshi et al. further teach that that the prescribed distance ranges from about 0.1 μm to about 5 μm (see col. 6, line 35 to col. 7, line 10).

As per claim 42, Joshi et al. further teach that the at least one silicon island includes a first silicon island including a single sensing and a single heating field effect transistor arranged a first prescribed distance apart, and a second silicon island including a single sensing and a single heating field effect transistor arranged a second prescribed distance apart (see col. 6, line 35 to col. 7, line 10).

As per claim 43, Joshi et al. further teach that the at least one heating field effect transistor is a first heating field effect transistor having a first number of contacts and a second field effect transistor having a second, different number of contacts, each configurable to generate heat arranged within the silicon island (see col. 3, line 64 to col. 4, line 30 and Fig. 4).

As per claim 44, Joshi et al. further teach that the calculating means calculates a temperature of the first heating field effect transistor and the second heating field effect transistor using the measured change in the at least one electrical characteristic and extrapolates results of the measurement to zero contacts (see col. 5, lines 36-55).

As per claim 54, Joshi et al. further teach arranging the first heating device and the first sensing device on an SiGe island; and using a common source contact which leads to the source of both the first heating device and the first sensing device (col. 4, lines 1-30 and col. 4, lines 40-67).

As per claim 55, Joshi et al. further teach arranging the heating transistor and the measurement transistor on an SiGe island; and using a common source contact which leads to the source of both the heating transistor and the measurement transistor (see col. 2, lines 55-67 and col. 4, lines 1-30; and col. 4, lines 40-67).

As per claim 56, Joshi et al. further teach that a heating gate contact being arranged on the silicon island and coupled to the transistor configured to generate heat; and a measurement gate contact being arranged on the silicon island and coupled to

the transistor configured to sense temperature (col. 4, lines 1-30 and col. 4, lines 40-67).

As per claim 57, Joshi et al. further teach a common source contact leading to the source of both the heating field effect transistor and the corresponding sensing field effect transistor (see col. 4, lines 1-30 and col. 4, lines 40-67).

Allowable Subject Matter

4. **Claims 19-23, 45 and 46** are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The following is a statement of reasons for the indication of allowable subject matter:

Regarding claims 19, 22 and 23, none of the prior art of record teaches or suggests calculating a temperature of the first heating device with the first number of contacts and the second number of contacts using the measured change in the at least one electrical characteristic, and extrapolating results of the measurement obtained with the first number of contacts and the second number of contacts to zero contacts, in combination with the rest of the claim limitations.

Regarding claims 20 and 45, none of the prior art of record teaches or suggests determining an offset between the first heating device and at least a second heating device, each having a different number of contacts, and extrapolating the offset to zero contacts.

Regarding claims 21 and 46, none of the prior art of record teaches or suggests the measurement step includes establishing an amount of temperature change per

contact between the first heating device and a second heating device having a different number of contacts and the calculating step includes extrapolating results of the measurement step to zero contacts to determine an actual device temperature without an offsetting effect of the contacts.

Response to Amendment

5. The Affidavit filed on 11/21/07 under 37 CFR 1.131 has been considered but is ineffective to overcome the Joshi et al. reference.

The evidence submitted shows no account for the entire period during which diligence is required. The entire period during which diligence is required must be accounted for by either affirmative acts or acceptable excuses. Applicant must account for the entire period during which diligence is required - MPEP 2138.06.

Applicant has only alleged that he has been diligent and has not provided evidence of facts establishing diligence.

Response to Arguments

6. Applicant's arguments filed November 21, have been fully considered but are not persuasive.

Applicant's arguments (pages 19-21) concerning the filing of a declaration under CFR 1.131 have been considered and are addressed above.

Conclusion

7. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Contact information

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Mohamed Charioui whose telephone number is (571) 272-2213. The examiner can normally be reached Monday through Friday, from 9 am to 6 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eliseo Ramos-Feliciano can be reached on (571) 272-7925. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Mohamed Charioui

2/14/08

/Eliseo Ramos-Feliciano/
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